Investigation of Ultra-Thin Gate Oxide Characterization and Establishment of Device Reliability Metrology in Deep-Submicron Processes

A Technical Report

By

Dr. Mu-Chun Wang

(王木俊 博士)

Department of Electronics Engineering
Minghsin University of Science and Technology

June 2005
Preface

From April, 1997 to August, 2001, the author served at United Micro-electronic Corporation (UMC) as a senior device manager. He dedicated to device characterization, reliability assessment, and electrostatic discharge damage (ESD)/Latchup investigation. The process technologies he joined were from 0.5um Al logic process to 90nm copper process. As he was an assistant professor at Da-Yeh University in 2001~2003, he also advised a UMC device engineer to study the 90 nm device characterization and the gate oxide reliability.

During the working era at UMC, he also had a chance to join the process development with IBM and Infenion from 0.18um to 0.13um generation. His main job function was the chief technical representative in reliability and device characterization. All of device test metrologies implemented into the auto testers were very impressed by the high-level chief officers at UMC because these tests would influence the mass production of the ICs and shorten the technology development time. How to provide the accurate, quick, and reasonable spec. as well as test methods was strongly desired. The author led a 7-person team and completed the annual assigned jobs. Moreover, during the working period, the total patents in this team, over 100 cases, were proposed. The published papers were 20. Due to all of UMC colleagues’ team work, the annual revenue of UMC was over NT$100 billion and the net profit was over NT$40 billion in 2000. This was a huge breakthrough in UMC’s history.

Owing to the eminent performance, not only IQ issues, but also EQ in cooperation and sharing, at UMC, as the author would resign, the senior VP F.T. Liu was not willing to sign his name on the resignation letter.

No doubt, because the author really contributed well in this area, the Tze-Chiang Foundation of Science & Technology (TCFST) invited him as a training lecturer from 1999 to 2005 and the submicron center at National Chiao-Tung University also invited him twice as the training speaker in reliability filed. The teaching courses, related to device measurement and reliability engineering, are over 10 times. He also had a chance to be a speaker at Power-Chip, TSMC, and AUO companies to present the process integration, semiconductor Physics, product reliability, and TFT device Physics, etc.

In this technical report, he will use over 30-patent contents and 10-published papers to integrate the ultra-thin gate oxide characterization and the device reliability concerns, including the test metrology and the test pattern design, etc. Furthermore, ESD/latchup effects will be explored, too. Some design concepts and fundamental research materials, excluding the commercial confidential information, have been employed in the teaching fields, seen in Appendix II. The related papers and patents are attached in Appendix III.
摘要

隨著半導體製程快速地演變，元件量測與元件可靠性效能也變得愈來愈有挑戰性。如何正確量得元件特性，特別是閘極氧化層的品質，以及設計合適的可靠性圖案作為偵測製程的好壞，已是個迫在眉睫的重大課題。當聯華電子從 1998 至 2001 時，在深次微米製程技術開發中，投入大量資金與人力又與其他大公司諸如 IBM, Infineon, Motorola, 及 AMD 等結盟時，若無此種度量工具與規格制定，則製程技術的開發將無所適從。

敝人在此關鍵時刻，被委任擔當此量測技術開發、量測規範的制定、與新監測圖案的設計重任。在深次微米製程技術中(一般指製程能力小於或等於 0.25 微米而言)，與 0.35 微米製程技術一比較，可以發現 0.25 微米或更先進製程技術有些重大革新，諸如在前段製程中元件的隔離方式，已由一般場氧化層改為淺溝槽隔離，而為了降低起動電壓($V_t$)值，開極複矽晶電極層也由单一電極植入改為雙電極植入;另一方面，開極氧化層為了適應雙電壓的 IC 設計需求，也採用雙開極氧化層厚度成長。而其他改變應用包括元件中的淺界面離子植入、短通道效應、表面通道傳導的考量等，都是非常重要的製程調整。在後段製程方面，也有些重大變革，例如高密度電漿化學氣相沉積、低介電係數材料的引進、銅製程技術也被廣泛使用等。

這些重大的演變，也牽動到元件模型的建立、元件的精細量測與特殊偵測圖案的設計、和元件可靠性工程的更新與新規格的探索，在在都須用心思考與反覆作實驗，以達到客戶可接受、可信任的製程。此技術報告，將以超薄氧化層($Tox \leq 50Å$)的特性研究，與新思維的可靠性量測建立，為重點著墨，並輔以靜電破壞性設計與閂鎖效應問題為探索。
Abstract

As the semiconductor process technology is tremendously evolved, the device measurement and the reliability performance become the challenging tasks. How to accurately measure the device characterization, especially in gate oxide quality, and design the suitable reliability patterns was a stringent issue as the deep-submicron process development plan at the United Microelectronic Corporation (UMC) in 1998–2001 was proposed.

In the deep-submicron process ($\leq 0.25 \mu m$), the process technology, comparing with the 0.35um process or above, has the big change such as the isolation replaced with shallow-trench isolation (STI), dual-poly-gate implants, dual-gate oxide, shallow junction consideration, surface channel conduction, low-k dielectric materials, copper process, and high-density plasma chemical vapor deposition, etc. At the same time, the developed devices also handled the huge challenge in worse short-channel effect, worse narrow width effect, stronger drain-induced barrier lowering effect, and higher stress-induced leakage, et al. Because of the previous statements, the device reliability in deep-submicron process faced the strong impact, too. Thus, the old reliability metrology applied to the deep-submicron process with 0.35um process generation or before was always questioned. As the author was the senior device manager at the technology development division/ UMC in 1998–2001, his main jobs covered to investigate the new measurement technology and the brand-new reliability assessment. Besides them, he also needed to cooperate with IBM and Infineon at the 0.18um and 0.13um complementary metal-oxide-semiconductor (CMOS) device reliability development and serve the reliability as well as the device characterization for Motorola and AMD, and so on. The chief conventional items in device reliability are the metal electromigration, the device hot-carrier effect, and the oxide reliability. The new generated device reliability issues such as the negative bias temperature instability at the positive metal-oxide-semiconductor device and the antenna effect are tremulous in the advanced process technology.

This technical report will focus on the gate oxide characterization, including the oxide thickness ($T_{ox} \leq 50$ Å) measurement, the tunneling effect, and the pattern design, and the discussion of the metrology of device reliability in test methods, spec. assessments, pattern designs, and ESD/latchup effects, etc.
Acknowledgement

The author, first, would like to give thanks to the Lord, Jesus Christ. He gave the author the wisdom and the humble heart, therefore, the author could complete the assigned jobs and co-work with colleagues well while the author stayed at UMC in 1997~2001. The other key persons such as the bosses, Dr. Y.J. Chang, Dr. K.Y. Fu, Dr. L. C. Hsia, Dr. Y.T. Lao, Dr. F.T. Liu, and Dr. M.C. Cheng, etc. are also appreciated due to their favors in administration and the supports in technical discussion. He also thanks all of his team members such as L.S. Huang, Dr. S.S. Chang, Howard Tang, U.C. Liu, Y.Y. Lin, S.C. Huang, and S.C. Kao. Because of their good devotion in the assigned jobs, the team performance was strongly recognized by the other group leaders. Furthermore, the author will give thanks to Dr. C.H. Liu and M.T. Lee, valued colleagues and friends. They not only shared their some ideas into this team, but also allowed the author to refer their data in this technical report. Some one ever gave the author some comments, suggestions, or special assistance at UMC. Here, the author thanks them, too. The author, especially, appreciates Professor Tahui Wang at NCTU for cooperating with UMC in ultra-thin gate oxide study and Professor M.D. Ker at NCTU in ESD protection design.

Finally, the author thanks his lovely wife due to her tender love and patience in this family and his smiling child, Daniel.
## Contents

I. Introduction .............................................. 06  
II. Gate Oxide Characterization ...................... 07  
   2-1. Fowler-Nordheim Tunneling .................. 07  
   2-2. Direct Tunneling ................................. 10  
   2-3. C-V Measurement ................................. 13  
   2-3-1. Conventional Test ............................. 13  
   2-3-2. Novel Extraction ............................... 18  
   2-4. C-F Measurement .................................. 26  
   2-5. Oxide Thickness Determination .............. 27  
   2-6. Statistical Investigation ....................... 31  
   2-7. Pattern Design for Gate Oxide ............... 34  
III. Device Reliability ................................. 41  
   3-1. Oxide Breakdown .................................. 41  
   3-1-1. Hard Breakdown in Gate Oxide ............. 42  
   3-1-2. Soft Breakdown in Gate Oxide ............ 47  
   3-1-3. Stress-Induced Leakage Current ........... 48  
   3-1-4. Method of Determining the Integrity of Ultra-thin Gate Oxide ........................... 50  
   3-2. Hot Carrier Effect ............................... 54  
   3-3. Negative Bias Temperature Instability ...... 62  
   3-4. Metal Reliability ................................ 64  
   3-4-1. Al Metal Reliability ......................... 64  
   3-4-2. Cu Metal Reliability .......................... 70  
   3-4-3. Antenna Effects ................................ 72  
   3-5. Crack Prevention in Low-k Assembly .......... 78  
   3-6. ESD/latchup Consideration .................... 79  
IV. Discussion ............................................. 90  
   4-1. Gate Oxide Characterization .................. 90  
   4-2. Device Reliability Consideration .......... 91  
V. Conclusion .............................................. 97  
VI. Reference ............................................ 99  
VII. Vita ................................................... 105  
VIII. Appendix I --- Awards and Service Events .... 107  
IX. Appendix II --- Teaching Experience ........... 109  
X. Appendix III --- Papers and Patents ............. 112